# 10016701\_CLS Most Frequently Occurring Classifications of Patents Returned From A Search of 10016701 on March 24, 2004

#### Original Classifications 714/726 16 714/731 8 6 714/727 3 714/733 2 324/73.1 2 365/233 Cross-Reference Classifications 714/724 7 714/733 714/30 4 714/736 365/201 714/727 3 714/732 2 327/202 2 714/726 714/731 Combined Classifications 18 714/726 10 714/731 10 714/733 9 714/727 8 714/724 5 714/736 4 714/30 4 714/732 3 324/73.1 3 \_ 365/201 2 327/202 2 365/233 2 714/718 2 714/738 716/4

10016701\_CLSTITLES
Titles of Most Frequently Occurring Classifications of Patents Returne

From A Search of 10016701 on March 24, 2004

18 n		.Digital logic testing	ERROR DETECTION/CORRECTION AND FAULT DETECTION/RECOVERY PULSE OR DATA ERROR HANDLING .Digital logic testingScan path testing (e.g., level sensitive sca			
1.0	714/701					
10		(8 OR, 2 XR) 714: ERROR DETECTION/CORRECTION AND FAULT DETECTION/RECOVERY				
	714/699 714/724	PULSE OR DATA ERROR HANDLING .Digital logic testing				
n	714/726	Scan path testing (e.g., level sensitive sca	ì			
	714/731	<pre>design (LSSD))Clock or synchronization</pre>				
10	714/733 Class 714/699 714/724 714/733	714: ERROR DETECTION/CORRECTION AND FAULT DETECTION/RECOVERY PULSE OR DATA ERROR HANDLING				
9			ì			
n	714/727	design (LSSD))Boundary scan				
8	714/724 Class	(1 OR, 7 XR) 714: ERROR DETECTION/CORRECTION AND FAULT DETECTION/RECOVERY				
	714/699 714/724	PULSE OR DATA ERROR HANDLING				
5	714/736	(1 OR, 4 XR)				

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	Class 714 714/699 714/724 714/736	10016701_CLSTITLES : ERROR DETECTION/CORRECTION AND FAULT     DETECTION/RECOVERY PULSE OR DATA ERROR HANDLING .Digital logic testingDevice response compared to expected     fault-free response			
4	714/30 (0 Class 714 714/100	: ERROR DETECTION/CORRECTION AND FAULT DETECTION/RECOVERY			
	714/1 714/25	.Reliability and availabilityFault locating (i.e., diagnosis or testing)			
g	714/27 714/30	Particular access structureBuilt-in hardware for diagnosing or testin			
-	4	within-system component (e.g., microprocess			
or t	est mode	circuit, scan path)			
4	714/732 (1 Class 714	OR, 3 XR) : ERROR DETECTION/CORRECTION AND FAULT DETECTION/RECOVERY			
	714/699 714/724 714/732				
3		OR, 1 XR) : ELECTRICITY: MEASURING AND TESTING PLURAL, AUTOMATICALLY SEQUENTIAL TESTS			
3	Class 365	OR, 3 XR) : STATIC INFORMATION STORAGE AND RETRIEVAL READ/WRITE CIRCUIT .Testing			
2		OR, 2 XR) : MISCELLANEOUS ACTIVE ELECTRICAL NONLINEAR     DEVICES, CIRCUITS, AND SYSTEMS SIGNAL CONVERTING, SHAPING, OR GENERATING .Particular stable state circuit (e.g.,			
	327/199	tristable, etc.)Circuit having only two stable states (i.e.,			
	327/202	bistable)Master-slave bistable latch			

		10016701 CLSTITLES
2	365/233 (2	2 OR, 0 XR)
	Class 365	5 : STATIC INFORMATION STORAGE AND RETRIEVAL
	365/230.01	ADDRESSING
	365/233	
	303/233	· bylic/ crocking
2	714/718 (3	OR, 1 XR)
_		: ERROR DETECTION/CORRECTION AND FAULT
	Class /1-	DETECTION/RECOVERY
	714/600	·
	714/699	
	714/718	.Memory testing
_	714/700	OD 1 VD)
2	714/738 (3	
	Class 71	ERROR DETECTION/CORRECTION AND FAULT
		DETECTION/RECOVERY
	714/699	PULSE OR DATA ERROR HANDLING
	714/724	.Digital logic testing
	714/738	Including test pattern generator
	, 11, , 50	
2	716/4 (3	OR, 1 XR)
	Class 71	5 : DATA PROCESSING: DESIGN AND ANALYSIS OF
	-	CIRCUIT OR SEMICONDUCTOR MASK
	716/1	CIRCUIT DESIGN
	716/4	.Testing or evaluating
	110/4	. restring or evaluating

## 10016701\_LIST PLUS Search Results for S/N 10016701, Searched March 24, 2004

The Patent Linguistics Utility System (PLUS) is a USPTO automated sear ch

system for U.S. Patents from 1971 to the present. PLUS is a query-by-example search system which produces a list of patents that a re

most closely related linguistically to the application searched. This search was prepared by the staff of the Scientific and Technical Information Center, SIRA.

### 10016701\_LIST

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5442640
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